Abstract

A semiconductor memory device includes a cell area; a predetermined cell block table for outputting the logical cell block address and the candidate information; and a tag block for receiving a row address, sensing a logical cell block address in the row address and outputting a physical cell block address based on the logical cell block address and the candidate information, wherein the tag block includes: a N+1 number of unit tag tables, each having M number of registers and storing a store information that the registers corresponds to M number of word lines, each register storing each the physical unit cell block address in response to the logical cell block among unit cell block addresses having a word line in response to the candidate information; and an initialization unit for initializing the N+1 number of unit tag tables.